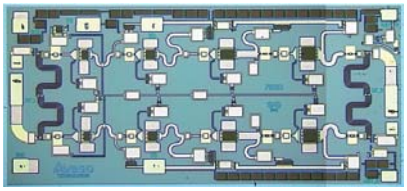
AMMC-6333

18 – 33 GHz 0.2 W Driver Amplifier

Data Sheet



Chip Size: 2500 x 1300 μm (100 x 51 mils)
Chip Size Tolerance: ± 10 μm (±0.4 mils)
Chip Thickness: 100 ± 10 μm (4 ± 0.4 mils)
Pad Dimensions: 100 x 100 μm (4 x 4 ± 0.4 mils)

Description

The AMMC-6333 is a broadband 0.2 W MMIC driver amplifier designed for use in transmitters operating in various frequency bands from 18 GHz to 33 GHz. This small, easy to use device provides over 23 dBm of output power (P_{-1dB}) and more than 20 dB of gain at 25 GHz. It was optimized for linear operation with an output power at the third order intercept point (OIP3) of 30dBm. The AMMC-6333 features a temperature compensated RF power detection circuit that enables power detection sensitivity of 0.3 V/W at 25GHz. It is fabricated using Avago Technologies unique 0.25μm E-mode PHEMT technology which eliminates the need for negative gate biasing voltage.

Features

- Frequency range: 18 to 33 GHz
- Small signal gain: 20 dB
- P_{-1dB} : 23dBm
- Return Loss (In/Out): -10 dB

Applications

- Microwave Radio systems
- Satellite VSAT, Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A) = 90 V
ESD Human Body Model (Class 1A) = 300 V
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Absolute Maximum Ratings

Symbols	Parameters	Unist	Maximum	Notes
Vd-Vg	Drain to Gate Voltage	V	14	
Vd	Positive Supply Voltage	V	5.5	
Vg	Gate Supply Voltage	V	0 to 5	
Id	Drain Current	mA	TBD	2
PD	Power Dissipation	W	2.5	2 and 3
Pin	CW Input Power	dBm	20	2
Tch	Operating Channel Temp	°C	+150	4
Tstg	Storage Case Temp.	°C	-65 to +155	
Tmax	Maximum Assembly Temp (30 sec max)	°C	+320	

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device. Functional operation at or near these limitations will significantly reduce the lifetime of the device.
2. Dissipated power PD is in any combination of DC voltage, Drain Current, input power and power delivered to the load.
3. When operated at maximum PD with a base plate temperature of 85 °C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures (Tj) be maintained at the lowest possible levels. See MTTF vs. Tchannel Temperature Table.

DC Specifications/ Physical Properties

Symbols	Parameters and Test Conditions	Units	Values
I_d	Drain Supply Current (V_d=5 V, V_g set for typical I_{dQ} – quiescent current)	mA	230
V_g	Gate Supply Operating Voltage (I_{dQ} = 230 mA)	V	2
I_g	Gate Supply Current	mA	7
$R_{\theta jc}$	Thermal Resistance (Channel-to-Backside)	°C/W	26
Tch	Channel Temperature	°C	115

Thermal Properties

Parameter	Test Conditions	Value
Maximum Power Dissipation	Tbaseplate = 85°C	PD = 2.5W Tchannel = 150°C
Thermal Resistance (θjc)	Vd = 5V Id = 230mA PD = 1.15W Tbaseplate = 85°C	θjc = 26°C/W Tchannel = 115°C
Thermal Resistance (θjc) Under RF Drive	Vd = 5V Id = 430mA Pout = 24dBm Pd = 1.89W Tbaseplate = 85°C	θjc = 26°C/W Tchannel = 134°C

MTTF vs. Tchannel Temperature

Operation	60% Confidence Level		90% Confidence Level		Point Data R=	
Tj	λ (ΦIT)	MTTF (hrs)	λ (ΦIT)	MTTF (hrs)	λ (ΦIT)	MTTF (Yrs)
150	3511	2.8E+05	8822	1.1E+05	3831	2.6E+05
140	1298	7.7E+05	3260	3.1E+05	1416	7.1E+05
130	456	2.2E+06	1147	8.7E+05	498	2.0E+05
120	152	6.6E+06	382	2.6E+06	166	6.0E+06
110	48	2.1E+07	120	8.3E+06	52	1.9E+06
100	14	7.0E+07	36	2.8E+07	15	6.5E+07
90	4	2.5E+08	10	1.0E+08	4	2.3E+08
80	1	9.9E+08	3	3.9E+08	1	9.1E+08
70	0	4.2E+09	1	1.7E+09	0	3.8E+09
60	0	1.9E+10	0	7.6E+09	0	1.7E+10
50	0	9.6E+10	0	3.8E+10	0	8.8E+10

RF Specifications

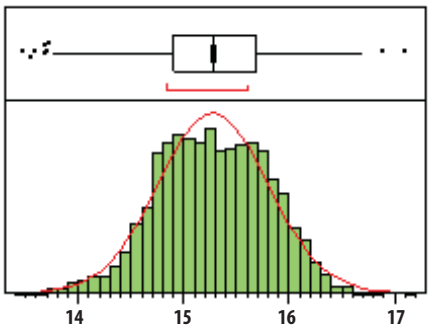
T_A= 25°C, V_d=5, $I_{d(Q)=}$230 mA, Z_o=50 Ω

			17 – 20 GHz			20 – 30 GHz			30 – 33 GHz		
Symbols	Parameters	Units	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
G	Small signal Gain	dB	13.5	17		17	22		15	20	
P_{-1dB}	Output Power at 1dB Gain Compression	dBm	19.5	23		20.5	23.5		21.0	23	
P_{-3dB}	Output Power at 3dB Gain Compression	dBm		23.5			24.5			23.5	
OIP3	Third Order Intercept	dBm		28			30			28	
RL_{in}	Input Return Loss	dB	8	10		13	14		13	10	
RL_{out}	Output Return Loss	dB	13	10		13	14		13	13	
	Reverse Isolation	dB		45			45			45	

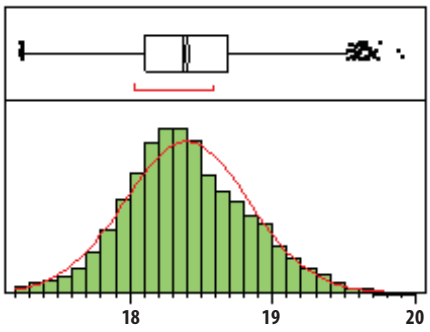
Note:
1. Measurements done on amplifier die attached to a metal carrier at T_A = 25°C.
2. 100% on-wafer RF test is done at frequency=17, 26 and 33GHz. Statistic based on 1500 part sample.

Product Consistency Distribution Charts

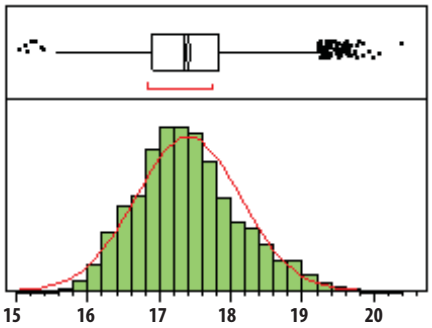
Typical distribution of Small Signal Gain and Output Power @P-1dB. Based on 1500 parts sampled over several production lots.



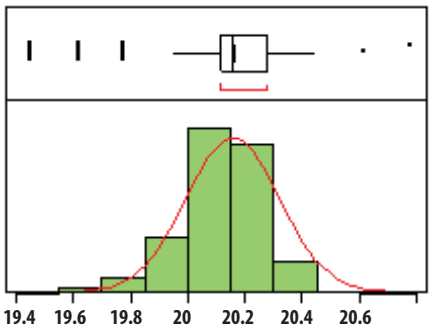
Gain at 17GHz



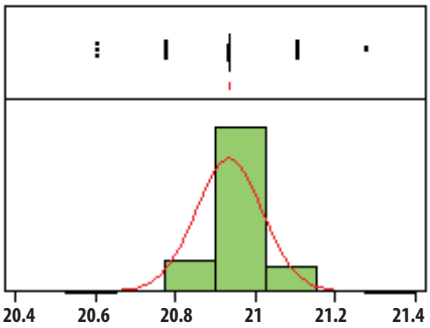
Gain at 26GHz



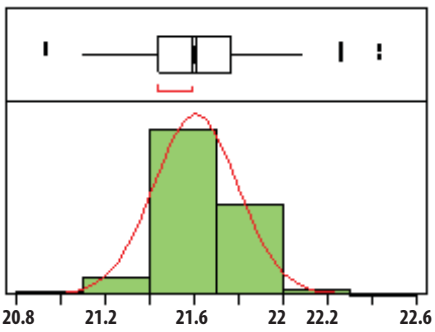
Gain at 33GHz



P1dB at 17GHz



P1dB at 26GHz



P1dB at 33GHz

Typical Performance

(T_A = 25°C, V_d =5 V, I_{dQ} = 230 mA, Z_{in} = Z_{out} = 50 Ω)

(Data obtained from a test fixture with 3.5 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

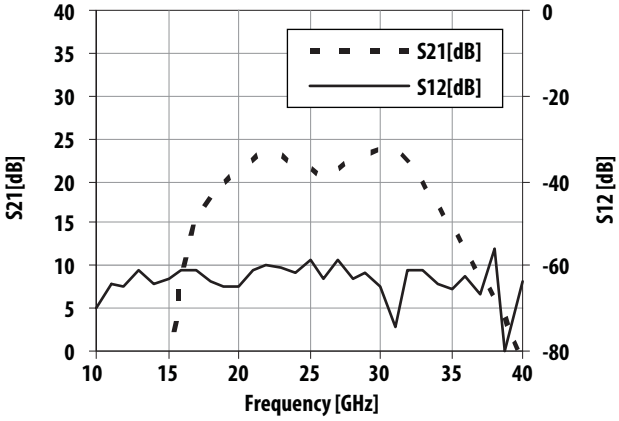


Figure 1. Gain and Reverse Isolation vs Frequency

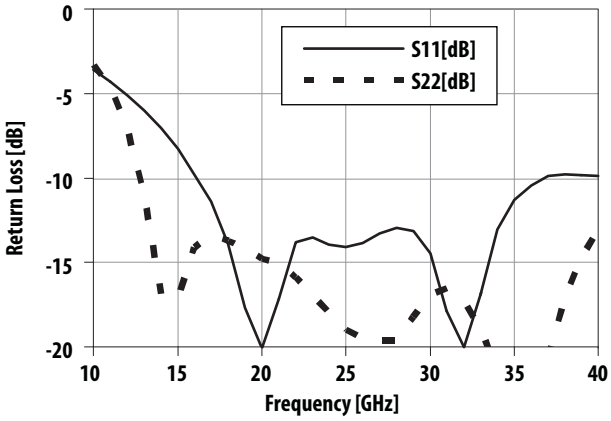


Figure 2. Return Loss vs Frequency

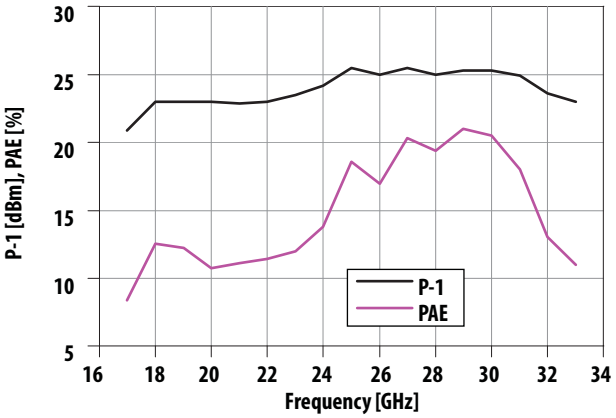


Figure 3. P-1dB and PAE vs Frequency

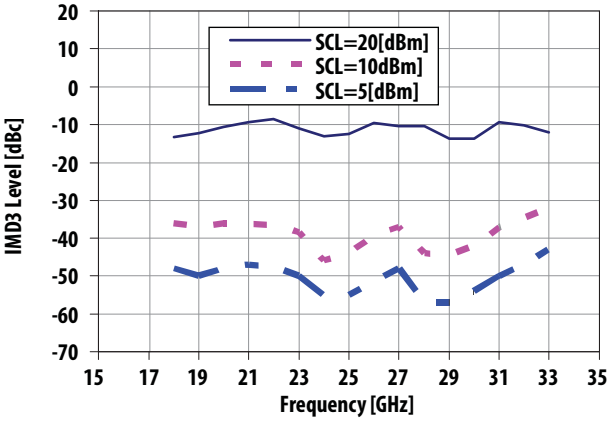


Figure 4. Typical IMD3 vs Frequency (SCL = Single Carrier level)

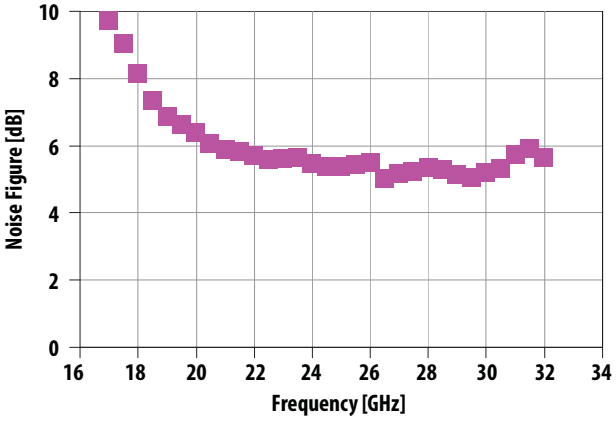


Figure 5. Typical Noise Figure vs Frequency

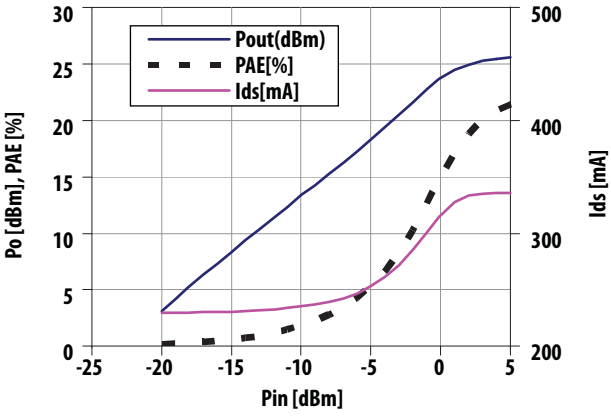


Figure 6. Output Power, PAE, and Drain Current vs Input Power at 30GHz

Typical Performance (continued)

(T_A = 25°C, Z_{in} = Z_{out} = 50 Ω)

(Data obtained from a test fixture with 3.5 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

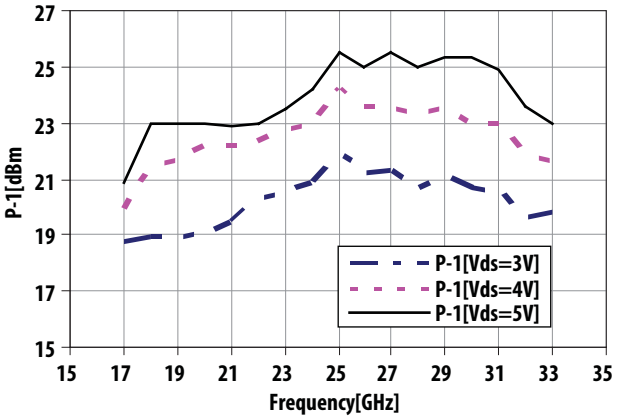


Figure 7. P_{-1dB} vs Frequency and Vds, (I_{dQ}=230mA)

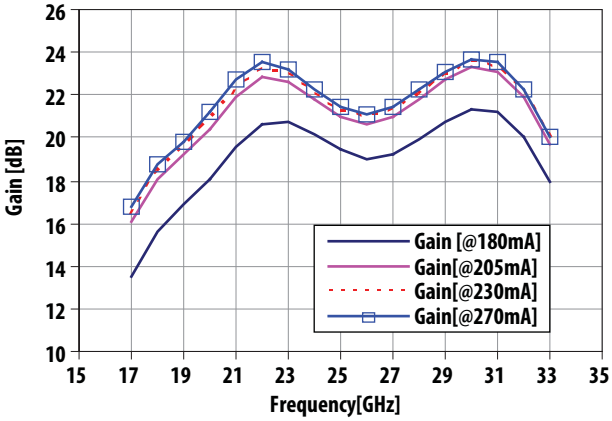


Figure 8. Small signal gain vs Frequency and I_{dQ}, (Vds=5V)

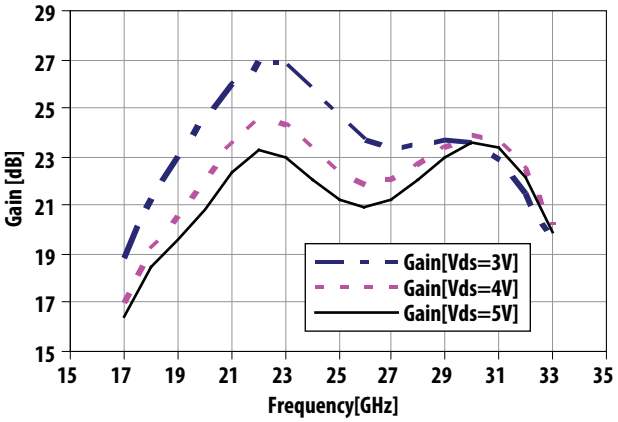


Figure 9. Small signal gain vs Frequency and Vds, (IdQ=230mA)

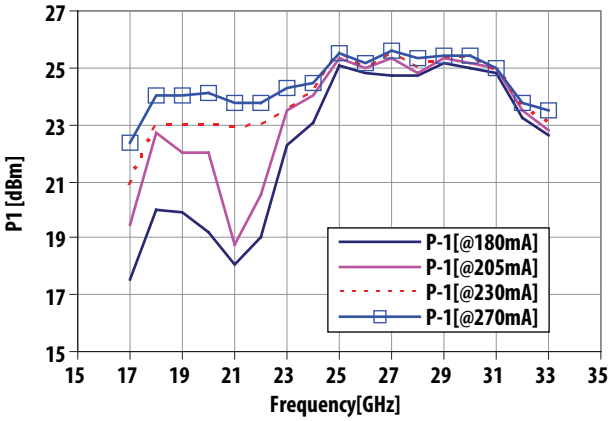


Figure 10. P_{-1dB} vs Frequency and I_{dQ}, (Vds=5V)

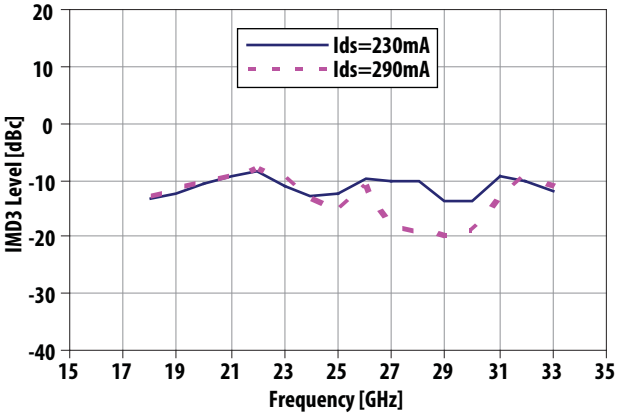


Figure 11. IMD3 levels vs Frequency
Fundamental output carriers at +20 dBm each

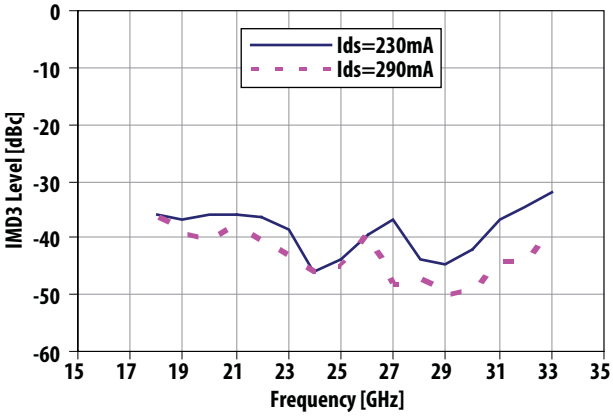


Figure 12. IMD3 levels vs Frequency
Fundamental output carriers at +10dBm each

Typical Performance (continued)

(V_d =5 V, I_{dQ} = 230 mA, Z_{in} = Z_{out} = 50 Ω)

(Data obtained from a test fixture with 3.5 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

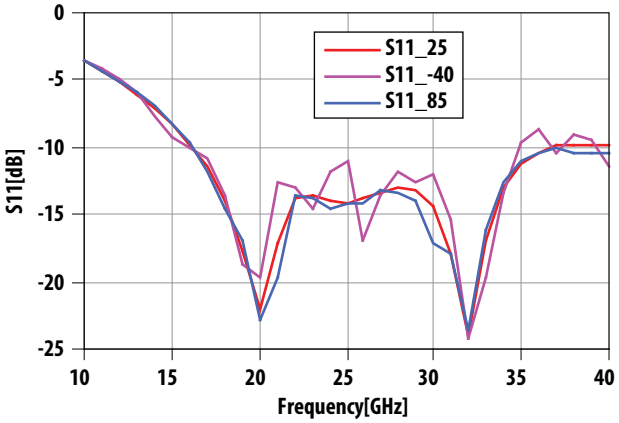


Figure 13. |S11| vs Frequency and Temperature

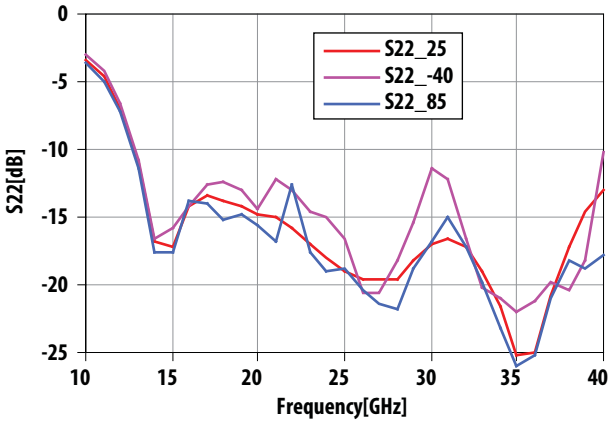


Figure 14. |S22| vs Frequency and Temperature

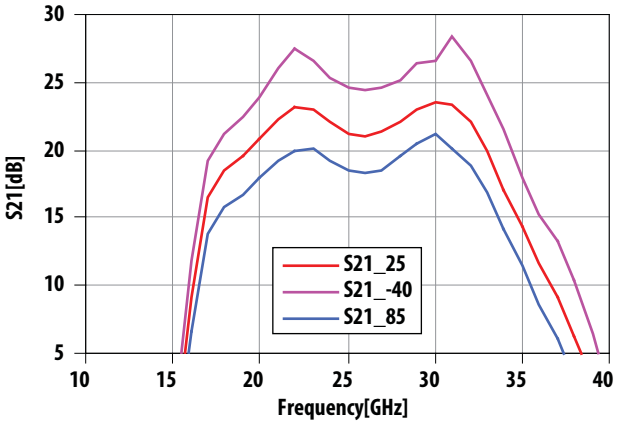


Figure 15. |S21| vs Frequency and Temperature

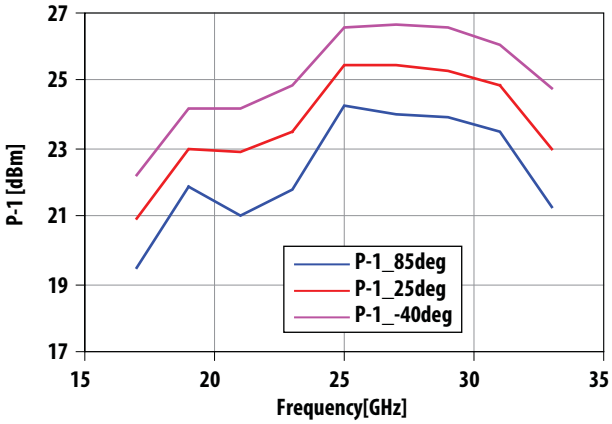


Figure 16. P_{-1dB} vs frequency and Temperature

Typical Scattering Parameters

(T_A = 25°C, V_d =5 V, I_{dQ} = 230 mA, Z_{in} = Z_{out} = 50 Ω)

Data obtained from on-wafer measurements

Freq	S11			S21			S12			S22		
[GHz]	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
1	-0.09	0.99	-19.89	-61.64	8.28E-04	-146.73	-74.90	1.80E-04	103.25	-0.04	1.00	-20.74
2	-0.21	0.98	-39.42	-62.28	7.69E-04	150.43	-75.57	1.67E-04	-150.10	-0.19	0.98	-41.30
3	-0.41	0.95	-58.86	-50.72	2.91E-03	-163.11	-67.84	4.06E-04	-66.78	-0.37	0.96	-61.20
4	-0.66	0.93	-77.74	-42.91	7.16E-03	125.53	-68.04	3.96E-04	-122.13	-0.65	0.93	-80.93
5	-0.99	0.89	-96.28	-39.71	1.03E-02	50.44	-65.33	5.41E-04	70.70	-1.09	0.88	-99.65
6	-1.37	0.85	-114.31	-41.23	8.68E-03	-25.35	-65.06	5.58E-04	17.92	-1.46	0.85	-116.58
7	-1.82	0.81	-131.80	-45.18	5.51E-03	-88.05	-66.55	4.71E-04	-93.35	-1.67	0.83	-133.89
8	-2.34	0.76	-148.79	-48.76	3.65E-03	-132.63	-68.24	3.87E-04	-146.85	-1.97	0.80	-152.22
9	-2.91	0.72	-165.32	-49.05	3.53E-03	-174.61	-64.71	5.81E-04	-165.57	-2.49	0.75	-171.38
10	-3.57	0.66	178.65	-46.39	4.79E-03	136.05	-70.17	3.10E-04	156.08	-3.32	0.68	168.61
11	-4.31	0.61	163.13	-42.34	7.64E-03	76.57	-64.27	6.12E-04	146.95	-4.67	0.58	147.60
12	-5.11	0.56	148.13	-40.22	9.75E-03	5.59	-64.65	5.85E-04	160.52	-6.99	0.45	126.34
13	-6.01	0.50	133.33	-34.51	1.88E-02	-164.12	-61.33	8.59E-04	110.59	-10.95	0.28	109.21
14	-7.03	0.45	118.85	-16.49	1.50E-01	104.02	-63.99	6.32E-04	70.70	-16.89	0.14	113.86
15	-8.27	0.39	104.82	-2.93	7.14E-01	28.77	-63.28	6.86E-04	86.57	-17.23	0.14	150.65
16	-9.77	0.32	91.48	9.17	2.87E+00	-60.34	-60.82	9.10E-04	56.53	-14.15	0.20	150.73
17	-11.39	0.27	78.76	16.48	6.66E+00	-173.35	-61.39	8.52E-04	52.15	-13.39	0.21	137.25
18	-13.91	0.20	66.29	18.45	8.37E+00	89.94	-63.36	6.79E-04	54.76	-13.75	0.21	128.38
19	-17.70	0.13	61.42	19.57	9.52E+00	11.09	-65.06	5.58E-04	61.87	-14.19	0.20	120.40
20	-21.98	0.08	87.84	20.85	1.10E+01	-59.74	-65.09	5.57E-04	41.98	-14.80	0.18	113.61
21	-17.19	0.14	115.36	22.32	1.31E+01	-129.79	-60.87	9.05E-04	52.67	-15.10	0.18	106.66
22	-13.80	0.20	99.41	23.25	1.45E+01	158.15	-59.62	1.05E-03	39.46	-15.89	0.16	99.42
23	-13.53	0.21	79.39	22.97	1.41E+01	87.48	-60.67	9.26E-04	1.30	-16.97	0.14	92.09
24	-13.98	0.20	70.02	22.06	1.27E+01	23.98	-61.62	8.30E-04	19.41	-18.02	0.13	87.64
25	-14.08	0.20	64.47	21.27	1.16E+01	-33.10	-58.47	1.19E-03	-34.32	-18.97	0.11	88.01
26	-13.85	0.20	55.72	20.93	1.11E+01	-86.92	-63.04	7.05E-04	-14.74	-19.50	0.11	88.84
27	-13.30	0.22	45.45	21.28	1.16E+01	-140.04	-58.66	1.17E-03	-40.94	-19.62	0.10	86.23
28	-12.97	0.22	31.03	22.07	1.27E+01	163.18	-63.21	6.91E-04	-55.59	-19.64	0.10	89.57
29	-13.18	0.22	12.01	22.94	1.40E+01	102.00	-61.82	8.11E-04	-71.10	-18.26	0.12	86.21
30	-14.46	0.19	-12.94	23.54	1.50E+01	35.50	-64.88	5.70E-04	-88.46	-16.95	0.14	73.26
31	-17.87	0.13	-50.60	23.36	1.47E+01	-35.54	-74.60	1.86E-04	-118.24	-16.54	0.15	53.38
32	-24.02	0.06	-147.39	22.16	1.28E+01	-108.19	-61.30	8.61E-04	10.40	-17.27	0.14	33.25
33	-16.94	0.14	120.38	19.91	9.89E+00	-178.81	-61.33	8.58E-04	-2.33	-18.91	0.11	9.85
34	-13.08	0.22	82.34	17.11	7.17E+00	115.36	-64.50	5.96E-04	-32.95	-21.56	0.08	-19.49
35	-11.31	0.27	58.07	14.36	5.22E+00	52.69	-65.79	5.13E-04	-13.39	-25.28	0.05	-64.03
36	-10.42	0.30	39.12	11.70	3.85E+00	-9.50	-62.25	7.72E-04	-41.34	-25.01	0.06	-133.57
37	-9.89	0.32	23.90	9.09	2.85E+00	-72.68	-67.00	4.47E-04	-169.14	-20.72	0.09	178.46
38	-9.77	0.32	9.70	6.28	2.06E+00	-139.02	-56.38	1.52E-03	-65.48	-17.20	0.14	147.77
39	-9.83	0.32	-1.34	2.77	1.38E+00	150.27	-82.42	7.57E-05	133.91	-14.70	0.18	124.20
40	-9.87	0.32	-10.26	-2.27	7.70E-01	79.17	-63.48	6.70E-04	-10.81	-13.07	0.22	104.19

Biasing Considerations

The AMMC-6333 is a balanced amplifier consisting of two four stage single-ended amplifiers, two Lange couplers, a power monitoring detector, a reference detector for temperature compensation, and a current mirror for the gate biasing (Figure 17).

The recommended quiescent DC bias conditions for optimum gain, output power, efficiency, and reliability are: Vd = 5 V with Vg set for I_{dQ} = 230 mA. The drain bias voltage range is from 3 to 5 V. Drain current range is from 200 mA to 350 mA. The AMMC-6333 can be biased with a dual or single positive DC source (Figure 18).

The output power detection network provides a way to monitor output power. The differential voltage between the DET_R and DET_O outputs can be correlated with the RF power emerging from the RF output port. This voltage is given by:

$V = (V_{DET\_R} - V_{DET\_O}) - V_{OFS}$

Where:

V_{DET_R} is the voltage at the DET_R port

V_{DET_O} is a voltage at the DET_O port

V_{OFS} is the offset voltage at zero input power

The offset voltage ($V_{OFS)}$ can be at each power level by turning off the input power and measuring V. The error due to temperature drift should be less than 0.01dB/50°C. When V_{OFS} is determined at a single reference temperature the drift error should be less than 0.25dB. Finally, V_{OFS} be characterized over a range of temperatures and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate V_{OFS} at any temperature.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

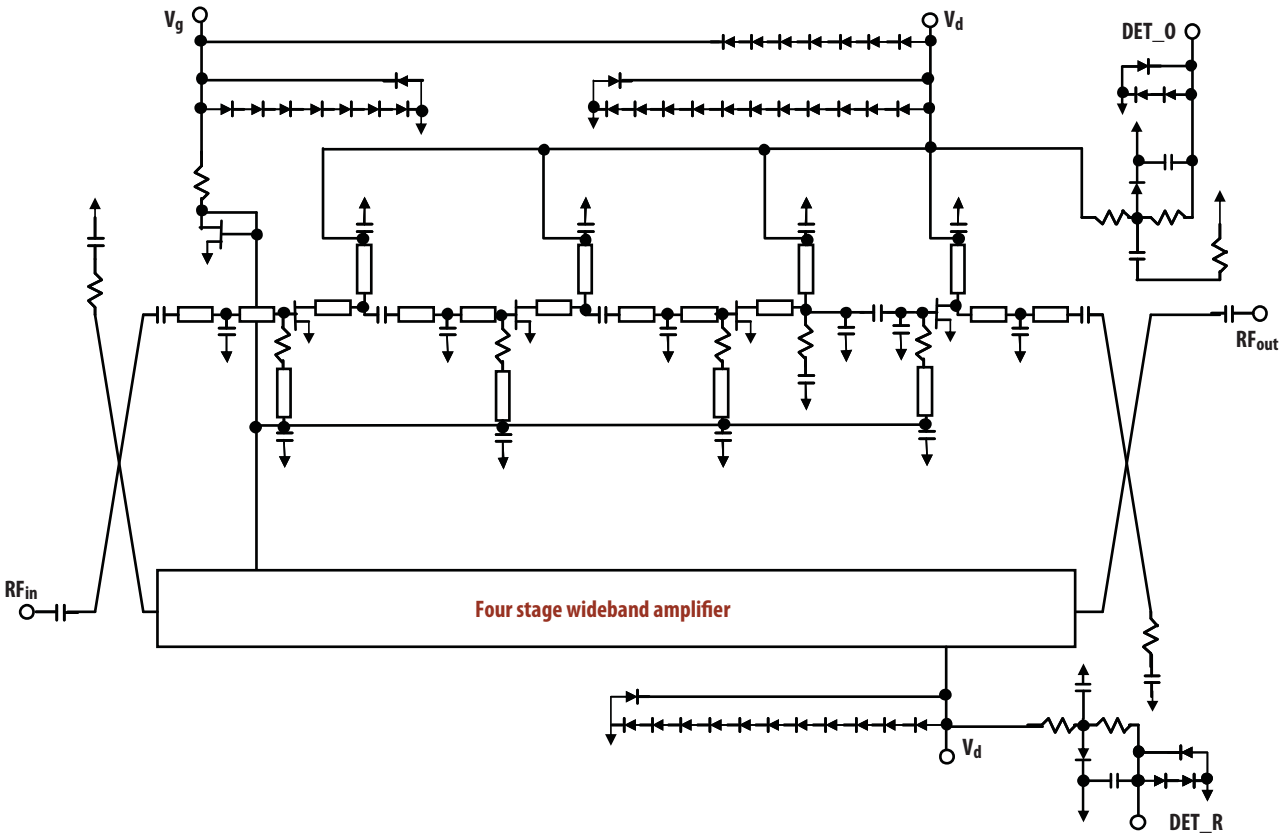
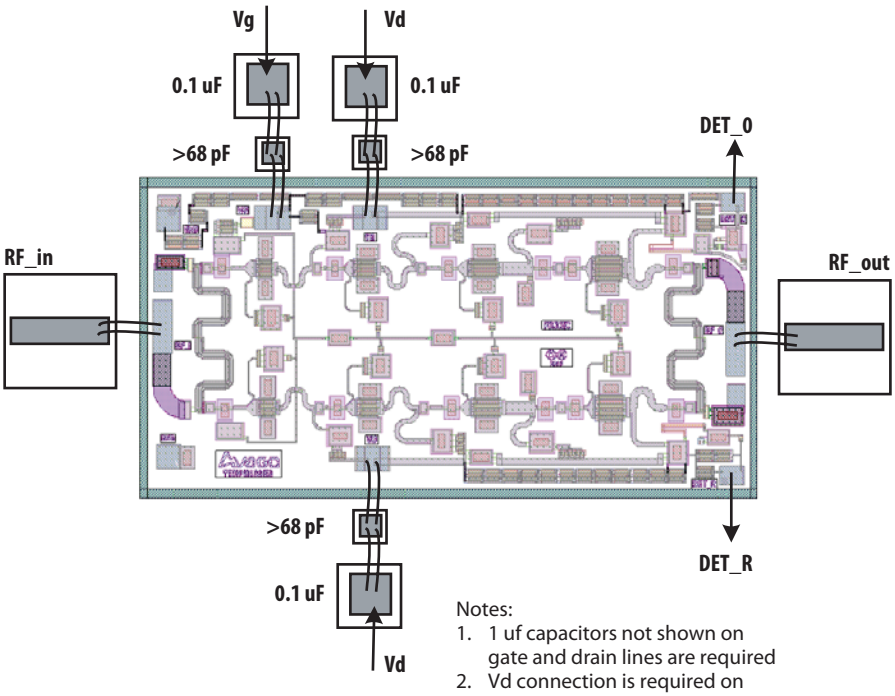
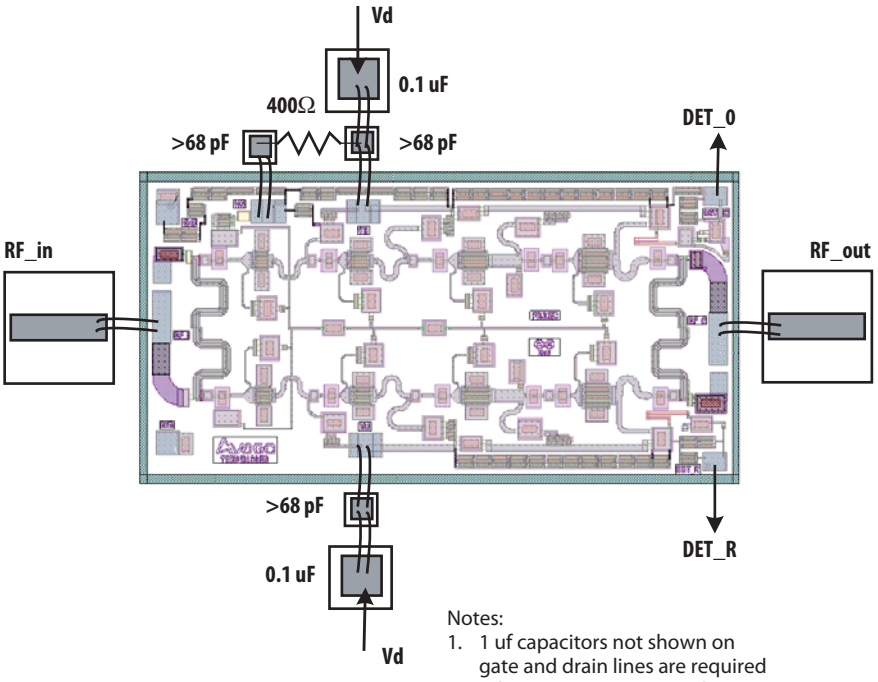


Figure 17. AMMC-6333 schematic



Notes:
1. 1 uf capacitors not shown on gate and drain lines are required
2. Vd connection is required on both sides

1. Dual positive DC power supply



Notes:
1. 1 uf capacitors not shown on gate and drain lines are required
2. Vd connection is required on both sides

2. Single positive DC power supply

Figure 18. AMMC-6333 biasing circuits

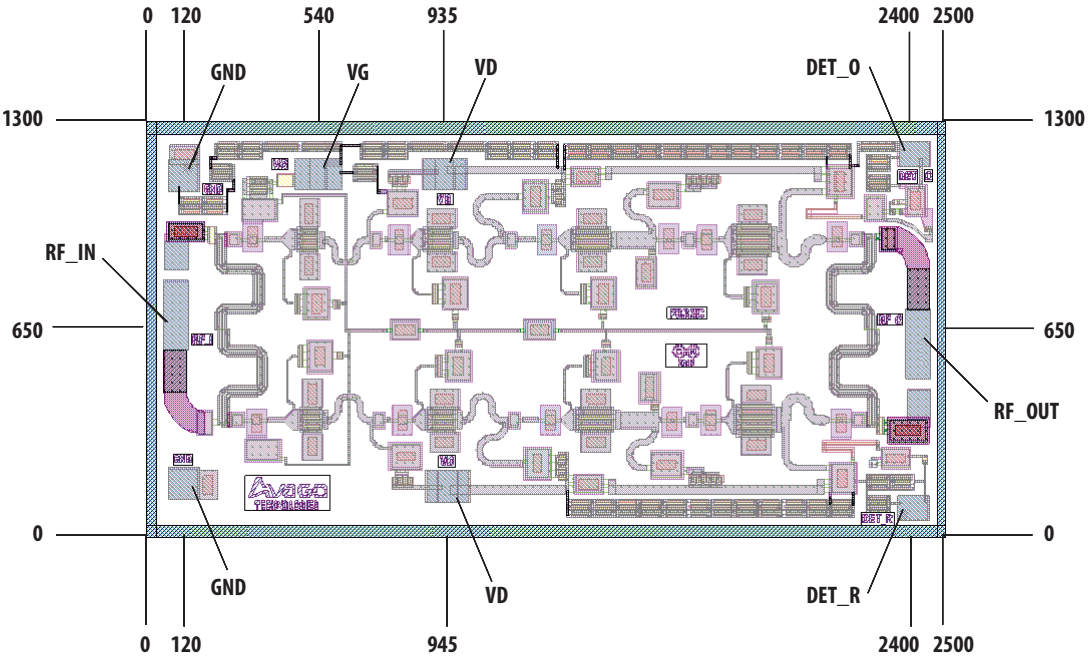
Assembly Techniques

The chip should be attached directly to the ground plane using electrically conductive epoxy (Note 1). For conductive epoxy, the amount should be just enough to provide a thin fillet around the bottom perimeter of the die. The ground plane should be free of any residue that may jeopardize electrical or mechanical attachment. Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

Thermo-sonic wedge bonding is the preferred method for wire attachment to the bond pads. The RF connections should be kept as short as possible to minimize inductance. Double-bonding with 0.7mil gold wire is recommended. The recommended wire bonding stage temperature is 150±2°C.

The chip is 100µm thick and should be handled with care. This chip has exposed air bridges on the top surface. Handle at the edges or with a custom collet, (do not pick up die with vacuum on die center).

This MMIC is static sensitive and ESD handling precautions should be taken.



Notes:
1. Ablebond 84-1 LM1 silver epoxy is recommended.

Figure 19. Die dimensions

Ordering Information:

AMMC-6333-W10 = 10 devices per tray
AMMC-6333-W50 = 50 devices per tray

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